WHAT IS CLAIMED IS:

1. A thin film transistor array substrate for a liquid crystal display, comprising:

a substrate;

a gate line assembly formed on the substrate to receive gate signals, the gate line assembly comprising gate lines proceeding in the horizontal direction, and gate electrodes connected to the gate lines;

a storage capacitor line assembly proceeding in the horizontal direction;

a gate insulating layer formed on the substrate while covering the gate lines and the storage capacitor line assembly;

a semiconductor pattern formed on the gate insulating layer over the gate electrodes;

a data line assembly formed on the gate insulating layer, the data line assembly comprising data lines crossing over the gate lines to define pixel regions, source electrodes connected to the data lines while being placed on the semiconductor pattern, and drain electrodes facing the source electrodes around the gate electrodes while being placed on the semiconductor pattern;

a protective layer covering the data line assembly and the semiconductor pattern, the protective layer having first and second contact holes; and

pixel electrodes formed on the protective layer at the respective pixel regions such that the pixel electrodes are connected to the drain electrodes through the first contact holes;

wherein the gate lines or the pixel electrodes are provided with repair members,

and the repair members partially overlap the front gate lines or the pixel electrodes.

2. The thin film transistor array substrate of claim 1, further comprising storage capacitor conductive patterns overlapping the storage capacitor line assembly while interposing the gate insulating layer, the storage capacitor conductive patterns being connected to the pixel electrodes through the second contact holes.

3. The thin film transistor array substrate of claim 1, wherein the parts of the gate lines overlapping the repair members are narrower than other parts.

4. The thin film transistor array substrate of claim 1, further comprising subsidiary repair members disposed between the repair members and the gate lines.

5. The thin film transistor array substrate of claim 4, wherein the subsidiary repair members are placed on the same plane as the data line assembly.

6. The thin film transistor array substrate of claim 1, wherein the storage capacitor line assembly comprises double storage capacitor electrode lines horizontally formed at the top and the bottom of each pixel region, and storage capacitor electrodes vertically formed at the periphery of the pixel region while interconnecting the storage capacitor electrode lines.

7. The thin film transistor array substrate of claim 1, wherein the repair member is formed with a ring shape.

8. The thin film transistor array substrate of claim 1, wherein the repair member is protruded from the pixel electrode.

9. The thin film transistor array substrate of claim 1, wherein the repair member is protruded from the gate line.

10. The thin film transistor array substrate of claim 1, wherein the volume of overlapping between the repair member and the front gate line, or between the repair member and the pixel electrode is ranged from $5\mu m^2$ to $1000\mu m^2$.

11. The thin film transistor array substrate of claim 1, wherein the semiconductor pattern has the same shape as the data line assembly except for the channel portion between the source and the drain electrodes.